REMARKS

Formal entry of this responsiv amendment as well as reconsideration and favorable action therefor on the present claimed subject matter is respectfully requested. (An authorized credit card payment form, covering the fee amount for the extended time period, is enclosed herewith.)

A new, substitute Abstract was provided to remove a discovered typographical error therein. Acceptance and formal entry therefor of the same is respectfully requested.

Independent claims 1 and 9 were revised in connection with further defining the insulating layer thickness of the thin-film transistor (TFT) covered by the claimed subject matter. In that regard, base claim 1 was amended so that it now incorporates the layer thickness previously set forth in dependent claim 2. Dependent claim 2, therefore, has been accordingly canceled. Independent claim 9 was amended so that it now calls for an "insulating layer" having a thickness defined by the range 4nm to 20nm. Regarding the layer thickness of the "first insulating layer" according to claim 1, this is discussed on page 9, lines 9-11, as well as in connection with the discussion on page 10 of the Specification regarding the relationship shown in Fig. 3 of the drawings. As to the layer thickness range of the insulating layer according to claim 9, as now amended, discussion regarding this is given from page 10, line 21, to page 11, line 2, of the Specification. Discussion will now turn to the art rejections.

According to the outstanding Office Action, claims 9 and 11 were rejected under 35 USC §102(b) as anticipated by Yamazaki et al (US 6,025,630); and claims 1, 2 and 22 were rejected under 35 USC §102(b) as anticipated by Abe et al (JP 8-195494). Regarding claim 2, the outstanding rejection directed thereto was rendered

moot with the canceling of that claim. It will b shown, also, hereinbelow, the inv ntion according to claims 1, 9, 11 and 22 could not hav been anticipated by Yamazaki et al nor by Abe et al nor, for that matter, rendered obvious even in view of their combined teachings. Therefore, insofar as presently applicable, these rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

According to independent claims 1 and 9 of the present invention, the "glass substrate" employed therein in connection with the formation of the thin-film transistor (TFT) has the physical property that "its compaction is 30 ppm or higher, when said glass substrate is heated at 600° C for 1 hour and thereafter cooled at a rate of 1° C/minute." Such, it is submitted, does not constitute a "product-by-process" limitation as that alleged in the outstanding rejections of those claims. That is, the invention according to claims 1 and 9 is not defined in terms of product-by-process limitations in which a glass substrate is actually annealed at a process temperature of 600° C as is alleged in the arguments of the rejection. Rather, these claims define a TFT scheme featuring, among other aspects thereof, a glass substrate having a specific physical property, namely, a property thereof in which the compaction (i.e., heat shrinkage) becomes 30 ppm or higher if annealed at a temperature of 600° C. This property is characteristic of the material employed in connection with the glass substrate. The specific limitation (in the claims) directed thereto does not stipulate whether or not the glass substrate is actually annealed at a temperature of 600° C. In other words, the glass substrate featured in independent claims 1 and 9 is such that a property associated therewith is necessarily of high compaction and a low density.

In accordance with the present invention, the TFT is implemented using a

polycrystalline silicon film in the formation of source, drain and channel regions to achieve greater electron mobility in the transistor over that employing, instead, an amorphous silicon layer. Applicants have achieved a scheme by which, also, the substrate strain point can be kept low thereby to avoid fluctuation in the threshold voltage as well as for the substrate to be inexpensively produced.

The present invention is based on the breakthrough finding making it possible to manufacture a TFT substrate even when a glass substrate having high compaction (in other words, a glass substrate that has not been previously annealed before a process) is used. This finding was achieved as a result of focusing on the relationship between that of the physical property and temperature of the glass, wherein an element is formed in the temperature range within which the compaction of the glass substrate does not adversely affect the properties of a TFT element even when the substrate is heated during the process. Accordingly, employing a glass substrate characterized by a compaction of 30 ppm or higher when the glass substrate is heated at 600° C for 1 hour and thereafter cooled at a rate of 1° C/minute defines an unannealed glass substrate. (Page 5, lines 8-14, of the Specification.)

As is apparent from the description of the TFT manufacturing technique described on pages 8-10 of the present Specification, it is evident that the glass substrate employed in a formation of the TFT of the first disclosed embodiment (e.g., see glass substrate 1 in Fig. 2[A]) is an "unannealed glass substrate CORNING 7059." Under such state, the glass substrate is characterized by a property of an exceedingly high compaction, namely, about 800 ppm, in connection with the above-mentioned heating process, namely, at a temperature of 600 ° C. However, as can be seen from the technique employed in the formation of the TFT of, for example,

the first embodim nt, a heat proc ss of around 450 ° C, which is substantially less than its upper limit and thereby significantly lowers th propensity for h at shrinkage, is employed in connection with the crystallization of the amorphous silicon material to yield a polycrystalline silicon layer. That is, upon providing an unannealed glass substrate as that presently called for, and employing a heat history of around 450 ° C in the process such as in Figs. 2(B) and 2(C) of the drawings, in connection with the example first embodiment disclosed, a thin-film transistor (TFT) such as shown in Fig. 1 which has stable characteristics and which is resistant to breakdown over time results.

According to claims 1+ and 9+, the invention therein calls for a thin-film transistor (TFT), an example of which is shown with regard to Fig. 1 of the present application, although not limited thereto. In accordance with the Fig. 1 example illustration, the transistor has an annealed glass substrate CORNING 7059 in the final structure, in which the glass substrate had been heated at about 450 ° C during the process. However, when the heat history is executed at a temperature of 600 ° C, the property of the glass under such condition provides an exceedingly high compaction. This is what is called as " a glass substrate having low compaction."

Abe was cited as, allegedly, disclosing the invention according to claims 1 and 22, insofar as presently applicable. Abe's semiconductor device scheme features a process of performing silicon oxidation in a steam atmosphere in which a glass substrate is made of CORNING 7059 glass. It is common knowledge, applicants submit, that a temperature should be about 700 ° C or higher to achieve an oxidation film on a silicon surface in a steam atmosphere, generally. Therefore, in order to be able to produce a thin-film transistor (TFT) using the above-mentioned process, a glass substrate such as CORNING 7059 should, however, be of the type having a

property of low compaction (or low heat shrinkage). In oth r words, an annealed glass substrate (i.e., a glass substrate having high density), which already has had a heat history at a temperature of 600 ° C or higher, should be employed in the process. Such would have been necessary in order for Abe et al to be able to achieve a low enough compaction. According to Abe's technique, it is submitted, it would only be possible to produce a transistor having stable properties if such an annealed glass substrate is used. A glass substrate having such a physical property, is completely different from that required according to the present invention, for the reasons noted hereinabove and as further described in the Specification.

Yamazaki et al ('630) disclosed a technique for achieving a thin-film transistor (TFT) employing a glass substrate (e.g., CORNING 7059) and a heating process such that the gate oxidation film is heated at a temperature of 550 ° C for an hour. The fact that the transistor can be manufactured without any trouble even after the glass substrate employed has already had a heat history of 550 ° C means that the glass substrate employed (CORNING 7059) already has a sufficiently small compaction property. That is, the glass substrate used by Yamazaki et al to achieve their invention is an annealed glass substrate (i.e., a glass substrate having high density), which has been previously processed with heat at a temperature of 600 ° C or higher. It is clearly apparent, therefore, the physical property associated with Yamazaki et al's glass substrate is completely different from that of the present invention.

To summarize, even though both the substrate of the present invention and that employed by both Abe et al and Yamazaki et al ('630) may be glass substrates of the CORNING 7059 variety, respectively, the physical property associated with

the glass substrate of the pres nt invention, howev r, is completely different therefrom. Th glass substrate characterized by the physical property called for in claim 1 and, therefore, also in dependent claim 22 and called for in claim 9 and the corresponding dependent claim 11 thereof is quite different from that taught by both Abe et al and Yamazaki et al. It is submitted, therefore, the invention according to claims 1+ and 9+ not only could not have been anticipated by either Abe et al nor by Yamazaki et al but, moreover, could not have been suggested even in view of their combined teachings.

In view of the amendments presented hereinabove, together with these accompanying remarks, formal entry therefor of this Amendment as well as favorable action on the presently pending claims, i.e., 1, 9, 11 and 22, and an early formal Notification of Allowability of the above identified application is respectfully requested.

If the Examiner deems that questions and/or issues still remain which would prevent the present application from being allowed at the present time, he/she is urgently invited to telephone the undersigned representative, at the number indicated below, so that either a telephone or personal interview may be arranged at the Examiner's convenience in order to discuss the same and hopefully resolve any remaining questions/issues present.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account of

Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (566.40894X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP

Larry N. Anagnos
Reg. No. 32,392

LNA/dks
703-312-6600

MARKED-UP VERSION SHOWING CHANGES MADE

IN THE CLAIMS:

Please **amend** claims 1 and 9 as follows:

1. (Twice Amended) A thin-film transistor comprising:

a glass substrate; and

formed at an upper part of said glass substrate, a channel region, a source region, a drain region, a first insulating layer and a second insulating layer, wherein:

said channel region, said source region and said drain region comprise polycrystalline silicon,

said glass substrate is such that its compaction is 30 ppm or higher, when said glass substrate is heated at 600° C for 1 hour and thereafter cooled at a rate of 1° C/minute,

said first insulating layer covers said channel region and has a layer thickness whose lower limit is 4nm, and

said second insulating layer is formed on a surface of said first insulating layer.

9. (Twice Amended) A thin-film transistor comprising:

a glass substrate; and

formed at an upper part of said glass substrate, a channel region, a source region, a drain region and an insulating layer, wherein:

said channel region, said source region and said drain region comprise polycrystalline silicon,

said glass substrate is such that its compaction is 30 ppm or higher, when said glass substrate is heated at 600° C for 1 hour and thereafter cooled at a rate of 1° C/minute, and

said insulating layer covers said channel region and has a layer thickness defined by the range 4nm to 20nm.

IN THE ABSTRACT:

Please **amend** the earlier submitted revised Abstract as follows:

ABSTRACT

To a polycrystalline silicon layer crystallized by irradiation with laser light, a mixed gas ~~comprises~~ comprised of ozone gas and H_2O or N_2O gas is fed at a processing temperature of 500°C or below, or the polycrystalline silicon layer is previously treated with a solution such as ozone water or an aqueous NH_3/hydrogen peroxide solution, followed by oxidation treatment with ozone, to form a silicon oxide layer with a thickness of 4 nm or more at the surface of the polycrystalline silicon layer for forming a thin-film transistor having characteristics that are less varying on a glass substrate previously not annealed.